Large >0.2dB/µm Modulation Depth Double-Layer Graphene Electro-Absorption Modulator on Slot waveguide

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Abstract: We experimentally demonstrated >10 dB extinction ratio (ER) at 4 V_{pp} with a 50µm-long double-layer graphene electro-absorption modulator (DLG EAM) integrated on a silicon slot waveguide. Both the modulation depth (0.2dB/µm) and efficiency (0.070 $dBV^{-1}µm^{-1}$) exceed state-of-art.

One of the most attractive properties of graphene is its strong, broadband, and tunable light absorption. Due to its atomic thickness, electro-absorption in graphene is best utilized when it is placed on top of an optical waveguide, so that the light interaction with graphene is controlled by waveguide length and mode overlap with the material. Recently several groups have reported high-performance and high bandwidth waveguide electro-absorption modulators (EAMs) operating with this principle [1,2]. The tradeoff between modulation efficiency and bandwidth needs to be considered when designing a graphene EAM. In most of the published work, the weak overlap of the optical field with the graphene layer results in low modulation efficiency, which requires relatively long devices reach a desired ER therefore increasing the device capacitance and reducing the speed. Accordingly, increasing the mode confinement in the graphene layer is key for realizing high-performance graphene modulators with optimized modulation efficiency and bandwidth [3]. In this work, we use slot waveguides to enhance light-matter interaction and we demonstrate a record high modulation depth of 0.2 dB/µm and modulation efficiency of 0.070 $dBV^{-1}µm^{-1}$ at CMOS- or BiCMOS-compatible drive voltages.

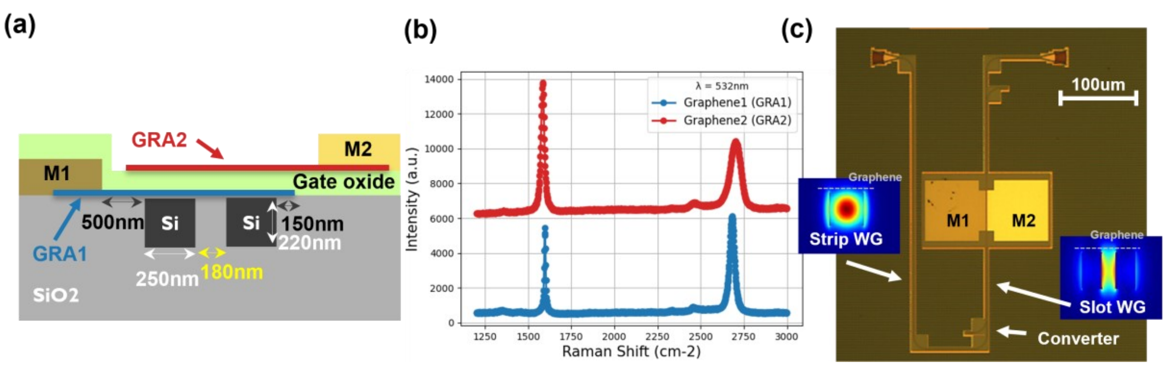

Fig. 1. (a) Schematic of DLG integrated on silicon slot waveguide with the optimized dimension taken from simulation. (b) Raman spectra of GRA1(blue) and GRA2(red) after device fabrication (c) Top-down microscope image of device with 50µm active length. The inserted TE modes are simulated by Lumerical.

The schematic cross-section of the proposed device is shown in Fig.1(a). The silicon waveguides were fabricated with standard modules in imec's CMOS pilot line. After surface planarization, the wafer was cleaved into pieces and the first layer of graphene, grown by Chemical Vapor Deposition (CVD) was transferred onto the cleaved substrate. Subsequently, E-beam lithography was used for graphene patterning and deposition of palladium contacts. It is an important step since both the dimension of the graphene layer and the distance between metal and waveguide edge will strongly influence the performance. After deposition of the gate oxide, the second layer of CVD Graphene (GRA2) was transferred, followed by similar patterning and metalization steps. Finally, Raman spectroscopy was used to characterize the quality of both Graphene layers, as shown in Fig.1(b). Both layers show a negligible D to G intensity ratio, indicating no significant degradation during the processing. Also, we can clearly observe a wider FWHM for the 2D peak in GRA2, which may be due to the strain induced in GRA2 from the topography created after GRA1 patterning and metal deposition. Fig.1(c) is the top-down view of the actual device. In our device, grating couplers are used for coupling light in and out of the chip. Furthermore, we add a mode converter between the strip and slot waveguide. As the mode profiles show in Fig1(c), the slot waveguides confine the light less in the Si region and the mode overlaps stronger with the graphene layers, enhancing the light-matter interaction.

Fig. 2 (a) shows the static spectral measurements in the C-band. First, the gate bias is normalized with respect to V_{Dirac}, i.e., the neutrality point of Graphene. Then the normalized transmission is plotted as function of this normalized gate voltage as seen in Fig. 2(b). The colored lines in this graph represent simulation results generated using a commercial mode solver (Lumerical™) for different graphene scattering times. We measured 4 dB additional loss between our experimental and simulation results, which attributed to the residues induced during our samples processing. After considering this extra loss, the measurements match well with the simulation results with ~11fs scattering time and 5nm equivalent oxide thickness (EOT). Both numbers are close to experimental results obtained from electrical test devices on the same chip. Fig. 2(c) shows the IL and ER for different V_{pp} from the previous graph. We define $V_{pp} = V_{large} - V_{small}$ and use V_{large} on the x-axis to comprehensively capture the device performance. For V_{pp} = 4V and V_{large} = 6V (V_{small} = 2V), the IL and ER are 9.2 dB and 10.4 dB, respectively, equivalent to a record-large modulation depth of~0.21dB/μm (compared to ~0.05 and ~0.1 dB/μm for earlier presented SLG and DLG [1] devices operating in the TE mode) and modulation efficiency ~0.070 $dBV^{-1}\mu m^{-1}$ (compared to ~0.038 $dBV^{-1}\mu m^{-1}$ for earlier DLG devices [2]), outperforming state-of art. The device can be further enhanced by improving the quality of graphene and processing. For example, simulations predict 1.4 dB IL and 12.8 dB ER at 4 V_{pp} for graphene scattering time of 44fs. Finally, the 3dB bandwidth was measured to be only ~2 GHz, which can be enhanced by improving the contact resistance, as well as by increasing the mobility and EOT. Our simulations show that for the same device size, 15nm EOT with 500Ωμm contact resistance and 44fs scattering time of graphene, the ER at 4V_{pp} can be increased to >6dB for >30GHz bandwidth. Therefore, this work illustrates how graphene can be used effectively for high-speed optical communication system.

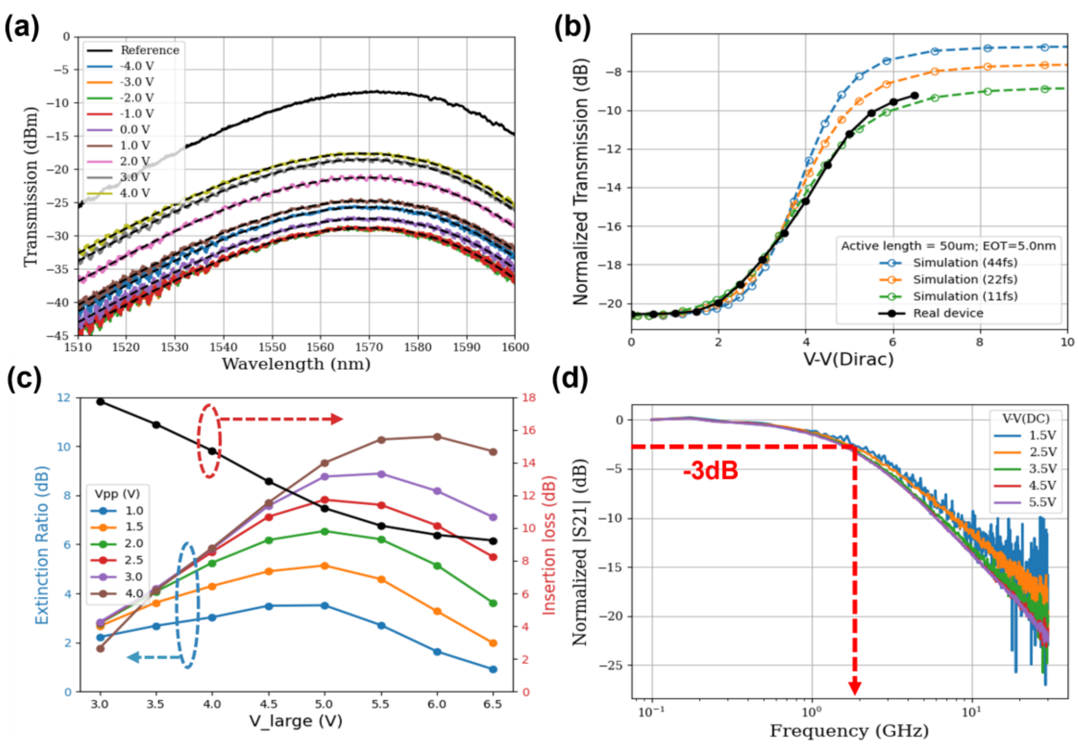

Fig. 2. (a) Transmission of the device with 50μm active length under different bias conditions. (b)Normalized transmission as a function of normalized gate bias. Filled and empty circles are experiment and simulation, respectively. (c) V_{large}-dependance of IL and ER extracted from Fig. 2(b). (d) S21 frequency response.

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